one second resistor value. The selective base epi region may comprise a SiGe base epi region.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-section through a prior art DIAC;

FIG. **2** is a cross-section through a prior art back to back NPN clamp with shared sub-collector;

FIG. **3** a circuit diagram of the clamp of FIG. **2**;

FIG. **4** shows a cross-section through one embodiment of an ESD protection circuit of the invention;

FIG. **5** shows a schematic circuit diagram of an ESD protection circuit of the invention;

FIG. **6** shows a top view of one embodiment of an ESD protection circuit of the invention, and

FIG. **7** shows a cross-section through another embodiment of an ESD protection circuit of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention defines a dual direction ESD protection circuit that can readily be adjusted to achieve different current-voltage (I-V) characteristics. In particular, the holding voltage and on-state resistance can be adjusted.

FIG. **4** shows a cross-section through one embodiment of an ESD protection circuit of the invention, which includes an NPN BJT that has two base-emitter fingers and a common sub-collector. The base-emitter fingers comprise a first emitter **400** and a first base **402** connected to a high voltage rail or pad **404**, and a second emitter **410** and second base **412** connected to ground **406**. The common sub-collector is defined by an N-epitaxial region **420**, which in this embodiment includes selective SiGe epitaxial regions to define SiGe base epitaxial regions below bases **402**, **412**. The SiGe base epi regions provide a bandgap that is different from pure silicon and allows for a very high speed NPN with Ft over 300 GHz. The remaining epitaxial region **420** is N-doped to define an N-epi sub-collector for the BJT. As shown in FIG. **4**, an n-buried layer (NBL) **422** is formed in the epi, leaving epitaxial region **424** below the NBL. The epi region **424** is p-doped. In this embodiment a first P+ region **430** is connected to the pad **404**. A second P+ region **432** is connected to ground **406**. By providing P+ regions **430**, **432** the BJTs are capable of adopting bipolar SCR (BSCR) characteristics as is discussed in greater detail below.

A schematic circuit diagram of the circuit of FIG. **4** is shown in FIG. **5**. The first emitter **400** and base **402** are connected to the pad **404**, while the second emitter **410** and base **412** are connected to ground **406**. As is shown in both FIG. **4** and the schematic of FIG. **5**, the first base **402** is connected to the pad **404** via a resistor **440**, and the second base **412** is connected to ground via a resistor **442**. The shared sub-collector region (N-epi **420**) is depicted in FIG. **5** by the connected collectors. The P+ region **430** formed in the N-epi defines a first diode **500**, while the P+ region **432** formed in the N-epi defines a second diode **502**, the P+ region **430** forming the anode of the first diode **500**, and the P+ region **432** forming the anode of the second diode **502**. The diodes **500**, **502** share a common cathode as defined by the N-epi and as depicted by the connection between the diodes **500**, **502** in FIG. **5**.

When a positive ESD pulse is applied to the pad **404**, the upper diode **500** is forward biased, thus providing a lower voltage on the collector of the upper NPN BJT **510** than the emitter **400** of NPN **510**. The base-collector junction of the lower transistor **512** is in turn reverse biased. At a certain voltage the base-collector junction of transistor **512** breaks down causing minority carriers in the base-collector junction, which allows current to flow through the upper diode **500** and the lower resistor **442**. The voltage drop across the resistor **442** opens the transistor **512**. The forward biased diode **500** provides additional injection of holes, which leads to the increase of the current and compensates for the space charge of carriers generated during avalanche multiplication in the base-collector junction, thus decreasing the holding voltage. By varying the level of additional injection of holes by the diode **500**, the current-voltage (I-V) curve of the clamp can be controlled. The level of injection in each direction can be varied in different ways, including by varying the number of P+ fingers per NPN BJT finger, by varying the distribution of P+ fingers among the BJT fingers, by varying the distance between the P+ region (finger or ring) and the BJT finger, and by varying the value of the base resistor **442** (for a positive ESD pulse) or resistor **440** (for a negative ESD pulse). By varying one or more of these parameters, the SCR effect can be enhanced or suppressed.

It will be appreciated that during a negative ESD pulse, the operation is similar to that discussed above except that current flow will be from the ground **406** through the diode **502** and the BJT **510**, using current flow through the resistor **440** to open up BJT **510**.

FIG. **6** shows a top view of one embodiment of an ESD protection circuit of the invention, which shows two different P+ region configurations. In this embodiment the ring-shaped P+ region **600** forms the anode of the upper diode **500** while the anode of the lower diode **502** is formed by a two P+ diffusion regions in the form of fingers **602**. The base-emitter fingers **604** are formed between the P+ fingers **602** in this embodiment.

Another embodiment of a dual direction ESD protection circuit of the invention is shown in FIG. **7**. Structurally it is similar to the circuit of FIG. **4** but the various regions are connected together differently to achieve different circuit performance.

The circuit of FIG. **7** again includes an NPN BJT that has two base-emitter fingers and a common sub-collector. The base-emitter fingers comprise a first emitter **700** and a first base **702** connected to a high voltage rail or pad **704**, and a second emitter **710** and second base **712** connected to ground **706**. The common sub-collector is again defined by an N-epitaxial region **720**. As in the embodiment of FIG. **4**, an n-buried layer (NBL) **722** is formed in the N-epi **720**. A first P+ region **730** is connected to the pad **704**. A second P+ region **432** is connected to ground **706**. By providing P+ regions **730**, **732** the BJTs are again capable of adopting bipolar SCR (BSCR) characteristics however, in contrast to the embodiment of FIG. **4** the P+ region (P+ SCR emitter region) is not adjacent to the base-emitter finger with which it forms a discharge circuit from pad to ground during a positive ESD pulse or from ground to pad during a negative ESD pulse. For example during a negative ESD pulse, the current path is defined by the P+ region **732** and the resistor **740** opening up the NPN BJT defined by the emitter **700** and base **702** with sub-collector **720**. The emitter **700** and base **702**, which are connected to the pad **704** are separated by a gap from the P+ region **732**, which is connected to the ground **706**. Thus the SCR effect is partly suppressed due to the larger gap between the P+ BSCR emitter **732** and the corresponding BJT finger of emitter **700** and base **702**. Similarly during a positive ESD pulse with current path through P+ region **730** and resistor **742** opening up the NPN